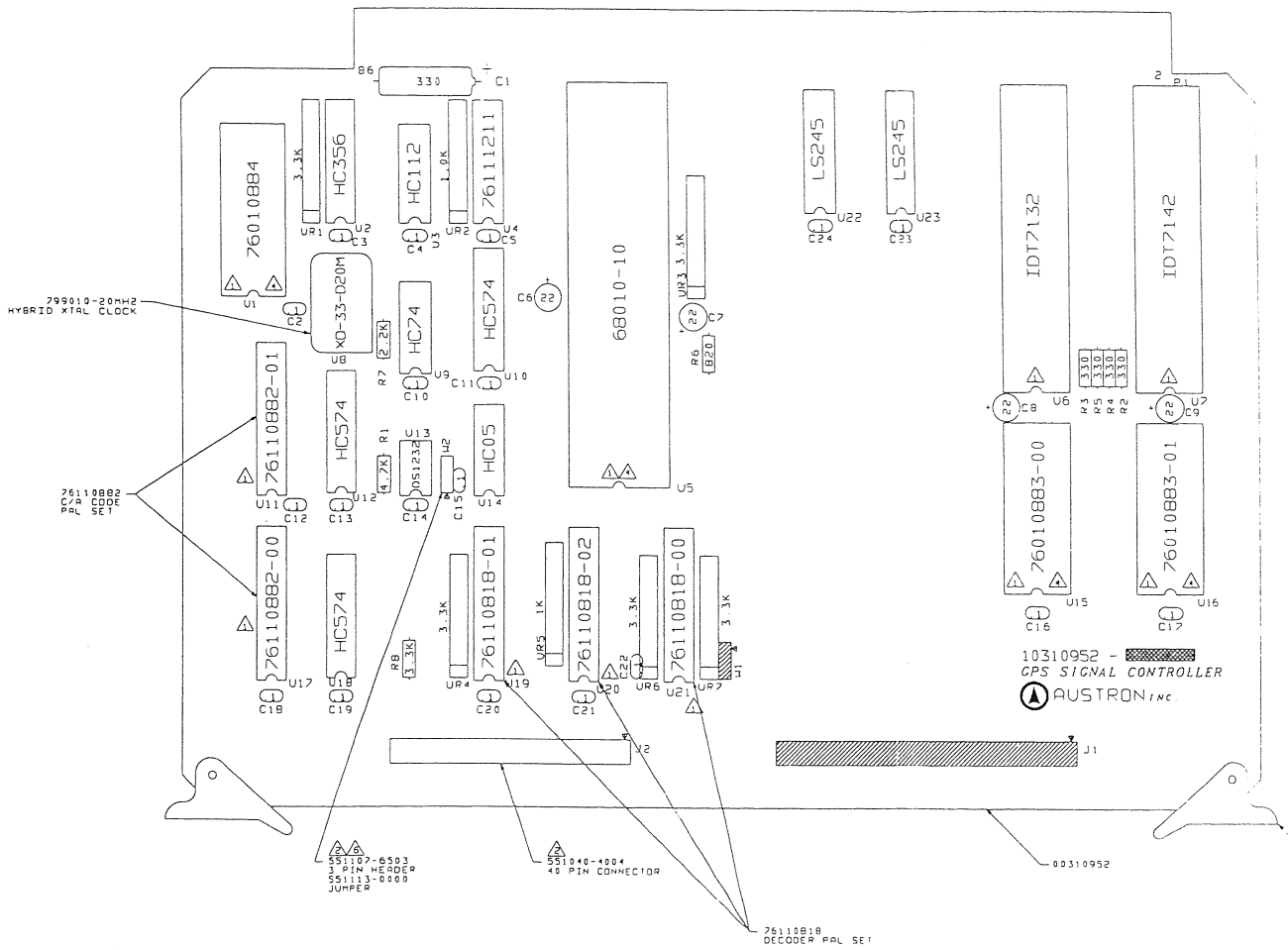
REVISIONS			
	A	RELEASED	
	B	U2 WAS NOT INSTALLED	



SOCKET LOCATION TABLE		
POS	PART NO	SIZE
U1 U15 U16	551016-0009	28
U6 U7	551016-0034	48
U5	551016-0035	64
U11 U12 U19 U20 U21	551017-0024	24

1. INSTALL JUMPER 551113-0000 ON PINS 2 & 3 OF U2 AFTER WAVE SOLDER.
2. ▨ INDICATES PART NOT INSTALLED ON PCB.
3. U1, U5, U15, & U16 ICs ARE INSTALLED BY TEST DEPT.; MFG INSTALLS SOCKETS ONLY.
4. STAMP REVISION LEVEL OF THIS DRAWING WHERE SHOWN.
5. INSURE ALL SOCKETS & CONNECTORS ARE MOUNTED FLUSH TO PCB.
6. WAVE SOLDER IC SOCKETS ONLY. INSTALL ICs AFTER WAVE SOLDER. REFER TO SOCKET LOCATION TABLE BEFORE INSTALLING SOCKETS.

NOTES:

NEXT ASSY	USED ON	REFERENCE DESIGNATOR	FIGURE NUMBER
2541:341	2203	A203	
2541:372	2203	A203	

APPLICATION

AUSTRON INC
A DATUM COMPANY

P.C.B. ASSY, GPS SIGNAL CONTROLLER

SIZE	DRAWING NO	REV
	10310952	B

SHEET 63

1.4.7. Signal Processor

Reference Dwg. No. 12310873 and Dwg. No. 10310873

The Signal Processor PCB contains the satellite signal sampling circuits, the C/A code clock circuit, the 1 pps generation circuit and the 10 MHz-to-10.23 MHz phase locked loop circuit. It is controlled by the Signal Controller PCB, and its primary function is to acquire and track satellites.

The satellite signal sampling circuits consist of the AGC circuit, the I and Q mixers, the I and Q samplers and the I and Q A/D converters. The third IF from the Antenna Interface module (rear panel) comes onto this board at P1-85,86. It is amplified and filtered by (U1B), op-amp high pass circuit, then sent to the input of the AGC circuit (U2,15).

The AGC circuit is controlled by the microprocessor to maintain a constant signal level. It does this by writing an 8-bit number, from 00 to FF, into latch (U3) whose eight outputs go to multiplying DAC (U2). When the D0 through D7 inputs of (U2) are all set to ones, the output of (U2) is approximately the same level as its input. As the number is decreased to 00, the output of (U2) decreases. IC (U1A) converts the current output of (U2) into a voltage and sends the third IF to (U9) and (U11).

Track-and-Hold ICs (U9) and (U11) are used here as mixers. Inphase and Quadrature signals (I and Q) from the Number Controlled Oscillator (U18) are connected to (U9) and (U11), respectively. They are at the same frequency as the third IF, and control whether the two ICs are tracking or holding. Because both the I and Q paths are electrically identical, only the upper path (I) will be discussed.

While the Hold input of (U9) is high, the IC holds the last value of the input. When it goes low, the output follows the input and goes to the low pass filter, consisting of R3 and C5. The filter removes the sum product of the mixer and passes the difference frequency. While the receiver is tracking a satellite, the difference frequency is kept at zero Hertz, leaving only the satellite data on the signal.

The output of the low pass filter goes to sample-and-hold (U16). Every millisecond, (U16) is placed in the Hold mode, holding the last voltage out of the filter. The sample-and-hold output goes to A/D converter (U26) where it is converted into a binary number. When the conversion is done, the A/D converter interrupts the microprocessor which then takes the data. The I and Q samples are the inputs to the software Costas loop which provides information for setting the NCO to keep the difference frequency at zero, provides information for setting the C/A code to keep the receiver tracking the satellite, and removes and filters the satellite data.

CAUTION: The NCO (U18) is an expensive CMOS IC. If it is ever necessary to remove this IC from the PCB, use extreme care to avoid damage from static electricity. It should be placed in a piece of conductive plastic while it is out of the board.

The C/A code clock circuit generates CACLK (U34,6), which clocks the 10-bit counter in the C/A code generator circuit on the Signal Controller PCB. Its frequency is 1.023 MHz and its phase can be shifted in steps of approximately 4 ns.

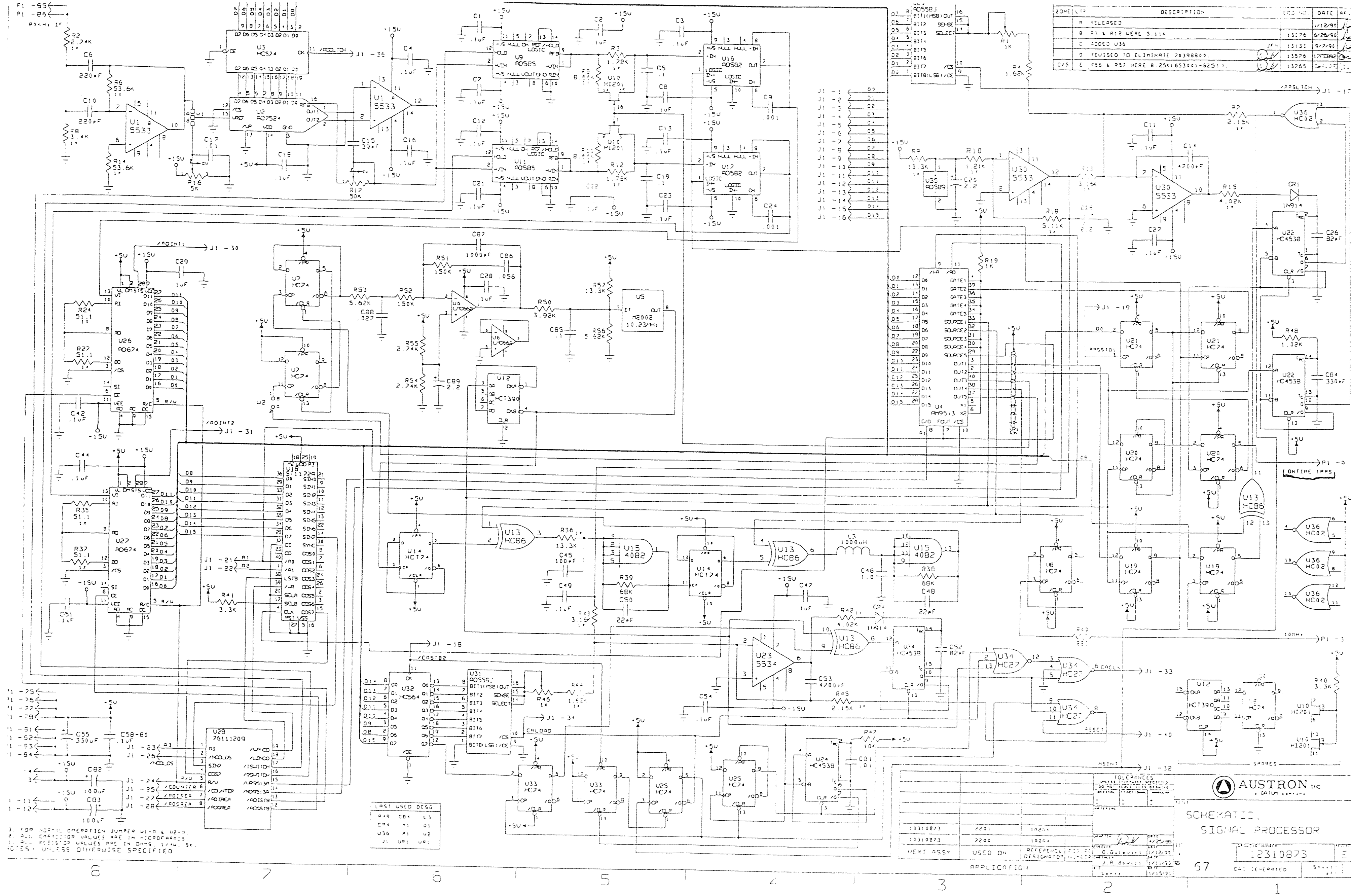
The microprocessor loads latch (U32) with a binary number that represents the amount of phase shift desired. The outputs of this latch go to the inputs of digital-to-analog converter (DAC) (U31). The voltage out of (U31) modifies the ramp rate of integrator (U23) to change the delay of one-shot (U24). When a change in phase is to be made, the microprocessor first enters the value in (U32). It then sets (U33,9) high, by generating the $\overline{\text{CASTB2}}$ strobe. This enables flip-flop (U25). Within 1 millisecond MSINT occurs, loading the new phase value. IC (U33) is cleared, causing both halves of (U25) to be cleared. Now the cycle can be repeated.

The 1 pps generation circuit consists of [(U4), (U19), (U20), (U21), (U22), (U29) and (U30)]. The microprocessor counts the millisecond interrupts (MSINT) and sets up counter (U4) when a 1 pps is to be generated. The 1 pps generation process begins when (U21,5) is set high by the microprocessor. This enables (U21) which is clocked on the next occurrence of the millisecond interrupt. IC (U21,9) goes high, enabling counter 2 of (U4). When counter 2 goes to zero, its output goes high (U4,2). On the next occurrence of the 1.023 MHz at (U20,11), (U20) is clocked, enabling (U20,2). On the next occurrence of the 1.023 MHz at (U20,3), a 1 pps is generated at (U20,5).

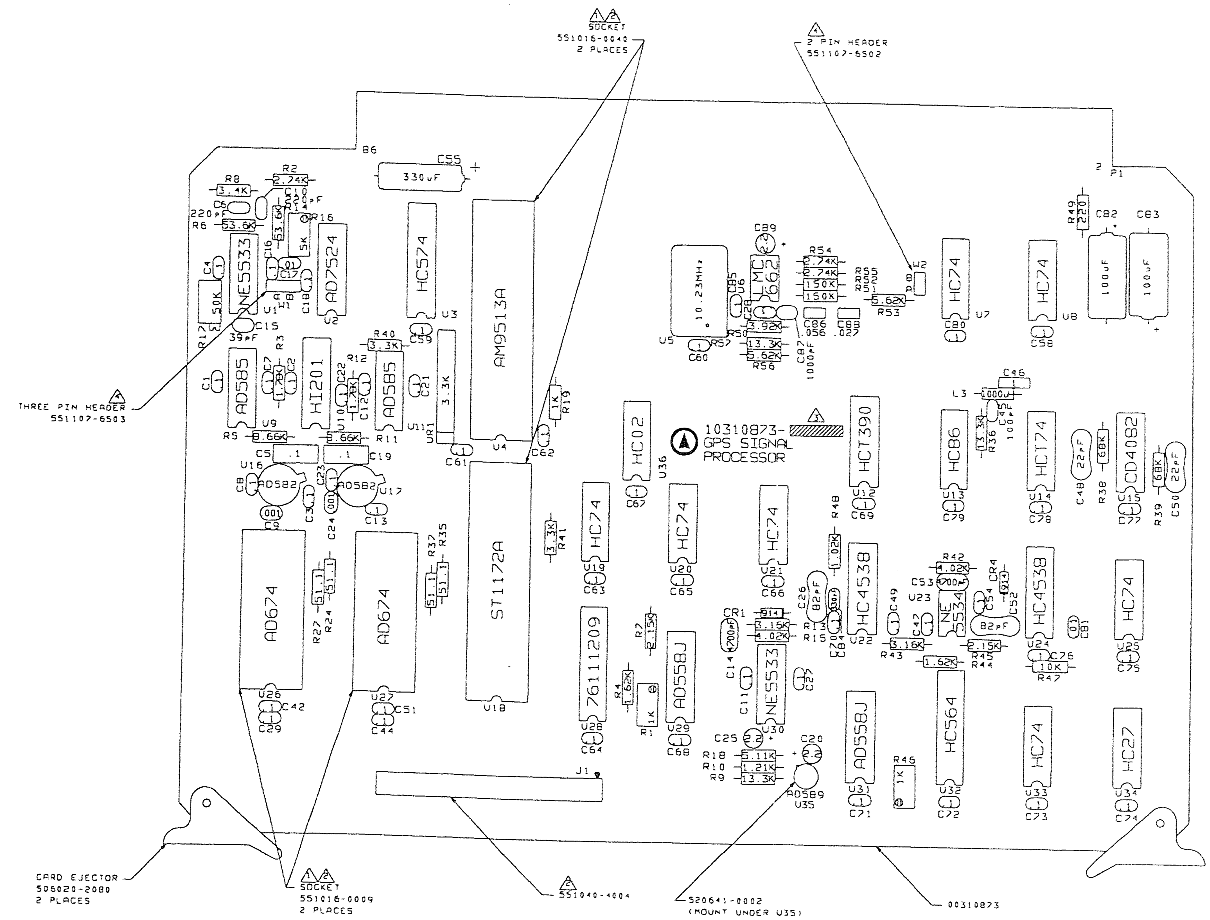
The delay of the 1 pps is changed by shifting the phase of the 1.023 MHz output at (U22,7) in steps of approximately 2 ns. This is done by changing the binary value of digital-to-analog converter (U29). The change in voltage at the output of the DAC changes the delay of the 1.023 MHz through one-shot (U22).

The 10.23 MHz phase locked loop phase locks the output of a 10.23 MHz oscillator (U5) to the internal 10 MHz reference. The 10.23 MHz output of the oscillator is divided-by-2 by flip-flop (U14). The 5.115 MHz output goes to (U13,2) which is part of a digital mixer. The other input of (U13) is 5 MHz. When these two frequencies are mixed, the output of (U13) has the sum frequency (10.115 MHz) and the difference frequency (115 kHz). Low pass filter, R36 and C45, remove the high frequency and pass the 115 kHz signal.

This signal is squared by (U15) and then divided by (U14). The resulting 57.5 kHz is mixed with 62.5 kHz, derived from the 10 MHz reference, in the second digital mixer [second gate in (U13)]. The difference frequency, 5 kHz, is passed by low pass filter, L3 and C46, and connected to one input of the digital phase comparator, [two flip-flops in (U7)]. The other input of the phase comparator is 5 kHz, derived from the internal 10 MHz. The $\overline{\text{Q}}$ output of (U7) is filtered and them applied to amplifier (U6) to produce a dc voltage for adjusting the frequency of the 10.23 MHz VCXO oscillator.


AUSTRON INC
A DATUM COMPANY
SCHEMATIC,
SIGNAL PROCESSOR
12310873
E
67
CAD GENERATED
APPLICATION
NEXT ASSY
USED ON
REFERENCE DESIGNATOR
12310873
2201
12310873
2200
ZONE
LTR
DESCRIPTION
DATE
A RELEASED
1/12/90
B R1 & R12 WERE 5.11K
13076
6/26/90
C ADDED U36
13133
9/7/90
D REVISED TO ELIMINATE 21398800.
13576
E R56 & R57 WERE 8.25K(653001-8251).
13765
LAST USED DESG
R49 C84 L3
CR4 Y1 Q1
U36 P1 U2
J1 UP1 UP1
3. FOR NORMAL OPERATION JUMPER W1-A & W2-A
2. ALL CAPACITOR VALUES ARE IN MICROFARADS
1. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.
NOTES: UNLESS OTHERWISE SPECIFIED
SPARES

REVISIONS					
ZONE	LTR	DESCRIPTION	ECO NO.	DATE	APVD
	A	RELEASED		1/12/90	
	B	R3 & R12 WERE 5.11K	13076	6/26/90	
	C	ADDED U36 JFM	13133	9/7/90	
	D	REVISED PER ECO TM	13244	9/7/90	
	E	REVISED OSCILLATOR CKT.	13576	17FEB92	
C/S	F	R56 & R57 WERE 8.25K	13765	26AUG92	
	G	REVISED PER ECO.	14057	15JUL93	



NOTE:

1. AFTER CLEANING PCB INSTALL JUMPER (551113-0000) IN LOCATION "A" ON W1, AND ACROSS PINS A & B ON W2.
2. STAMP REVISION LEVEL OF THIS DRAWING WHERE SHOWN.
3. INSURE ALL SOCKETS & CONNECTORS ARE MOUNTED FLUSH TO PCB.
4. WAVE SOLDER IC SOCKETS ONLY. INSTALL IC's AFTER WAVE SOLDER.

NEXT ASSY	USED ON	REFERENCE DESIGNATOR	FIGURE NUMBER
25411941	2201	1A2A4	
25410972	2200	1A2A4	

APPLICATION

TOLERANCES UNLESS OTHERWISE SPECIFIED
DO NOT SCALE THIS DRAWING

DRAFTER: Don W. — 3/5/88
CHECKER: D. Gulawski — 1/12/90
ENGINEER: J. R. Bowell — 1/11/90
Q.C.: Lopez — 1/15/90

AUSTRON INC
a DATUM company

TITLE: PCB ASSY, SIGNAL PROCESSOR

DRAWING NUMBER: 10310873 — REVISION: G

69

CAD GENERATED — Sheet 1 of 1

1.4.8. Antenna Interface Module (A3A8)

Reference Dwg. No. 23411147, Dwg. No. 12310732 and Dwg. No. 10310732

The Antenna Interface module amplifies and filters the first IF from the antenna, generates the second and third IFs, and removes the C/A code. The resulting nominal 80 kHz is filtered and amplified and sent to the Signal Processor PCB.

The first IF (75.42 MHz) from the antenna enters the module at J1. It is amplified by amplifiers (U13) and (U14), then sent to mixer (U12). At (U12), the 75.42 MHz is mixed with a 90 MHz signal which has been phase modulated by the C/A code in mixer (U9). At the output of (U12), the remaining signal of interest is the second IF, approximately 14.58 MHz, which still has the Doppler and the satellite data on it. This signal is amplified by (U15), then sent to the crystal filter which consists of Y1 and Y2. The filter removes the unwanted mixer components and some of the noise.

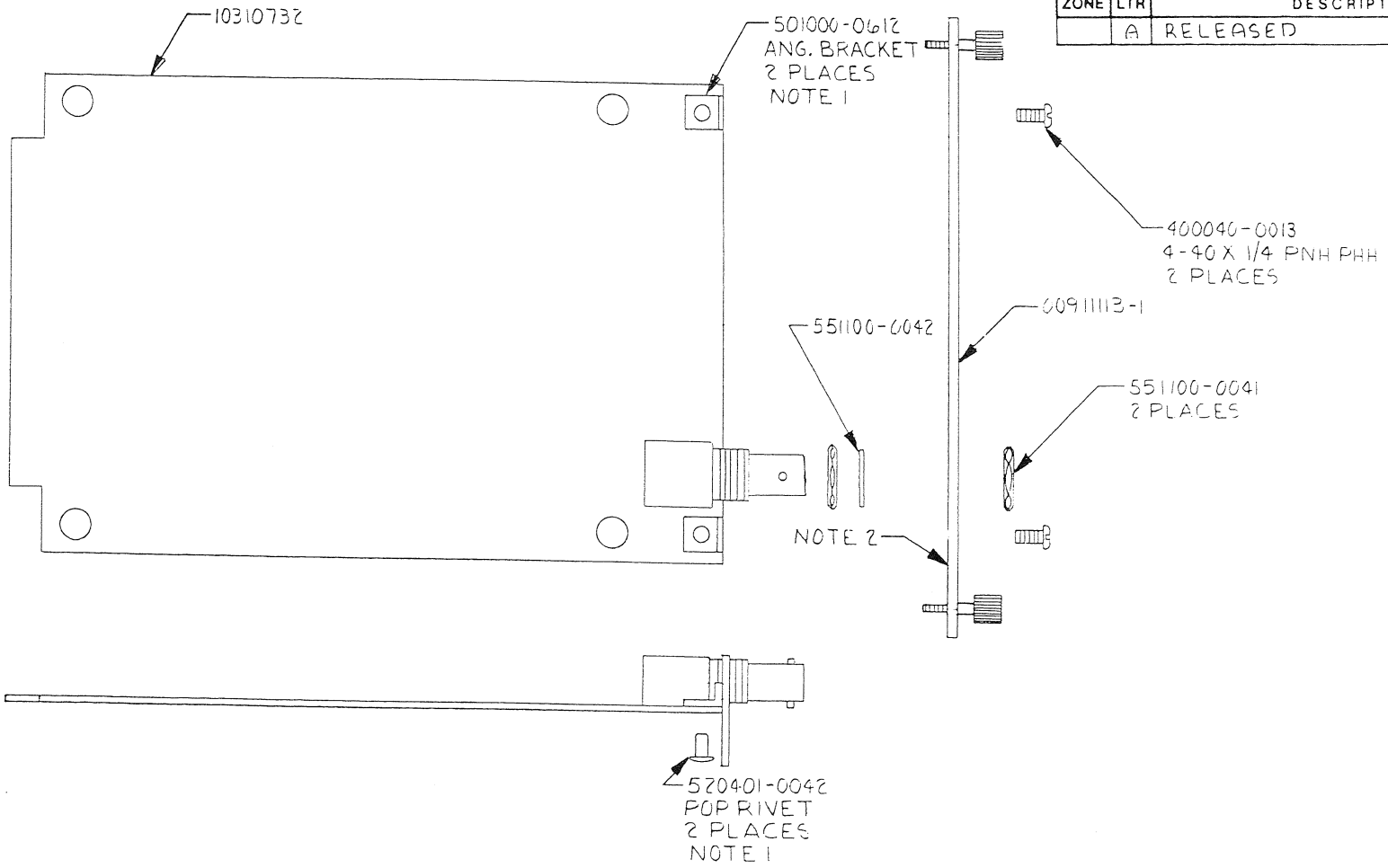
The signal is further amplified in (U8), then sent to mixer (U4). Here it is mixed with 14.5 MHz from (U3). The 14.5 MHz is generated by mixing 15 MHz, obtained by dividing the 30 MHz output of (U7) by 2, with 500 kHz, obtained by dividing the 10 MHz reference by 20 in divider (U5). The sum and difference signals (15.5 MHz and 14.5 MHz) are amplified by (U3) and connected to mixer (U4).

The products obtained by mixing 14.58 MHz with 15.5 MHz and 14.5 MHz are 30.08 MHz, 0.92 MHz, 29.08 MHz and 80 kHz. Op-amp (U1) amplifies these products (mostly the 80 kHz), then sends them to the active filter formed by the second half of (U1). The bandwidth of this filter is approximately 7 kHz, centered at 80 kHz. Only the 80 kHz component of the last mixing is passed by this filter. Its output is then sent to the Signal Processor.

Inductor, L5, connects the 15 volts to J1. This inductor prevents the first IF (75.42 MHz) and the 10 MHz reference from getting onto the power supply. It also keeps these signals from being shorted out by the low impedance of the power supply. The low pass filter, composed of L15-L17, C31 and C32, filters the 10 MHz reference before it is connected to J1.

NOTES:

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	A	RELEASED	12/22/89	gm



25411941	2201			
25410972	2200	1A3A8		
NEXT ASSY	USED ON	REF DES	FIG NO.	
APPLICATION				

TOLERANCES
UNLESS OTHERWISE SPECIFIED

DEC	FRAC	ANG

MATERIAL:

Q.A.	Copied	1-9-90
ENGR	KRS	12/22/89
CHECK	gm	12/22/89
DRAWN	[illegible]	10/20/87

AUSTRON INC.
AUSTIN, TEXAS

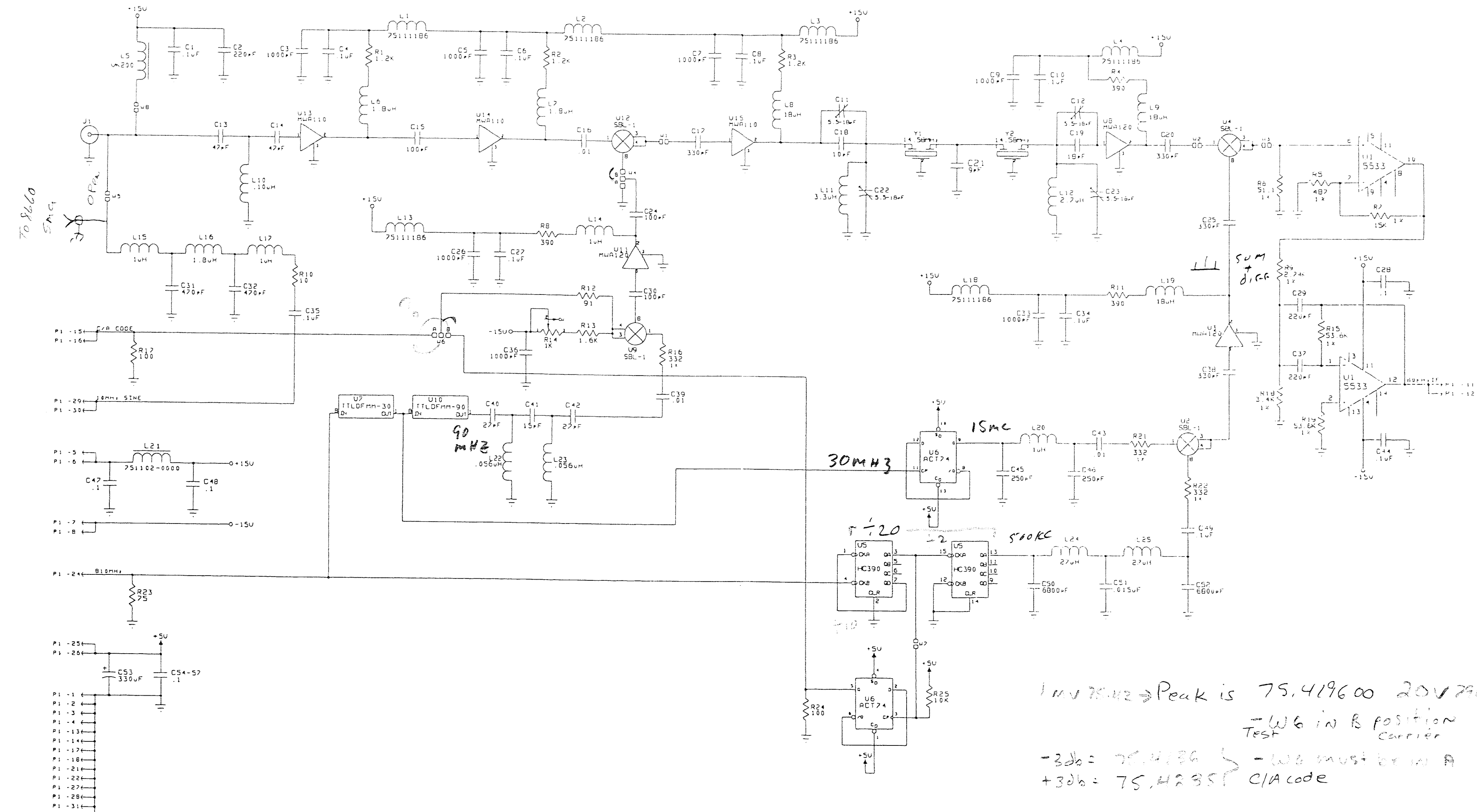
MODULE, ANTENNA INTERFACE

SIZE	CODE IDENT NO.		REV
2	73 P2	23411147	A
SCALE		SHEET 1 OF 1	

2. STAMP P/N & APPROPRIATE REV ON UNPAINTED SIDE OF PANEL.
1. RIVET ANG. BRACKET TO PCE FIRST.

NOTES:

ZONE	LTR	DESCRIPTION		DATE	
	A	RELEASED			



3. JUMPERS W1, W2, W3, W4-B, W5, W6-A, & W8 ARE CLOSED FOR NORMAL OPERATION.
2. ALL CAPACITORS HAVE VALUES IN MICROFARADS
1. ALL RESISTORS ARE 1/4W, 5%, WITH VALUES IN OHMS.
NOTE: UNLESS OTHERWISE SPECIFIED—

POWER & GND CHART

REF DESG	GND	VCC	BYPASS CAP
U5	8	16	C54
U6	7	14	C55
U7	7	14	C56
U10	7	14	C57

LAST USED REF DES

R25	C57	L25
U15	J1	P1
Y2	W8	

NEXT ASSY	USED ON	REFERENCE DESIGNATION	FIGURE NUMBER
10310732	2201	1A3A8A1	
10310732	2201	1A3A8A1	

APPLICATION

AUSTRON INC. A DATUM COMPANY

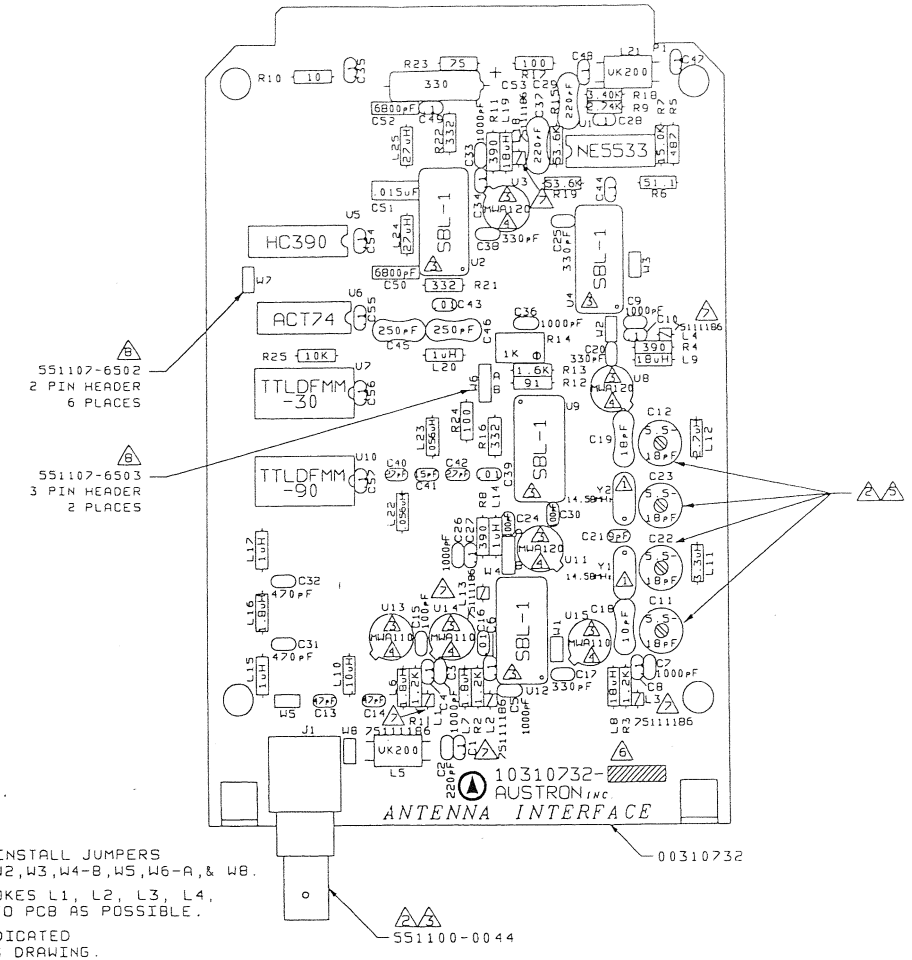
SCHEMATIC, ANTENNA INTERFACE

12310732

75

OSC 9.9999988 5345 10SEC

REVISIONS					
ZONE	LTR	DESCRIPTION	ECO NO.	DATE	APVD
	A	RELEASED		1/1/90	JH
	B	REV PER ECO 13188 P/L ONLY Jm	13188	12/4/90	JH



△8 AFTER CLEANING PCB, INSTALL JUMPERS (551113-0000) ON W1,W2,W3,W4-B,W5,W6-A,& W8.

△7 MOUNT SUPPRESSION CHOKES L1, L2, L3, L4, L13, & L18 AS CLOSE TO PCB AS POSSIBLE.

△6 STAMP BOARD WHERE INDICATED WITH REV. NO. OF THIS DRAWING.

△5 DO NOT CLEAN C11,C12,C22, & C23 IN VAPOR DEGREASER. CLEAN W/ALCOHOL ONLY.

△4 INSTALL XTSR PAD (511010-0006) BETWEEN XTSR & PCB AT U3,U8,U11,U13,U14, & U15.

△3 MOUNT ALL SBL-1's,MWA120's,MWA110's, & J1 FLUSH TO PCB.

△2 INSTALL J1,C11,C12,C22, & C23 AFTER WAVE SOLDER.

△1 Y1 & Y2 (754000-0001) ARE A MATCHED SET. DO NOT MIX PARTS WITH OTHER SETS.

NOTE: UNLESS OTHERWISE SPECIFIED --

23411147	2201	1A3AB1	
23411147	2200	1A3AB1	
NEXT ASSY	USED ON	REFERENCE DESIGNATOR	FIGURE NUMBER
APPLICATION			

TOLERANCES UNLESS OTHERWISE SPECIFIED DO NOT SCALE THIS DRAWING
DECIMAL ± FRACTIONAL ± ANGULAR ±
MATERIAL
DRAFTER Don W. DATE 5/11/88
CHECKED DATE 12/4/90
ENGINEER DATE 12/4/90
Q.C. DATE 12/5/90

AUSTRON INC AUSTIN, TEXAS

TITLE
P.C.B. ASSY, ANTENNA INTERFACE

SIZE 3 | DRAWING NUMBER 10310732 | REVISION B
SCALE 14:9 | 77 | CAD GENERATED | Sheet 1 of 1

2. Maintenance

2.1. Scope Of Section

Section Two provides the technician with a general approach to maintaining the Model 2201A. Included are trouble analysis guides and general maintenance procedures. Refer to Section One for detailed functional descriptions of the various circuits.

2.2. Trouble Analysis Guide

Considerable lost time and trouble can be avoided by following certain steps before beginning any major troubleshooting procedure. If the Model 2201A is malfunctioning and general testing is in order, go through the following checklist before starting the tests.

1) AC and dc connections on the rear panel are secure.
2) Receiver is connected to a functional power source.
3) AC fuse is intact and dc circuit breakers are not tripped.
4) Required external signals are connected to the receiver.
5) The antenna is properly installed, and the antenna cable is tightly secured at the antenna and the ANTENNA input on the Antenna Interface module.
6) It is sometimes helpful to clean the contacts of the PCBs. To do this, remove all power connections to the receiver. Carefully remove each PCB, lightly clean both sides of the edge-connector with a typewriter eraser or alcohol and return it to the slot from which it was taken.

If the problem still exists after performing the checks listed above, it will be necessary to run more extensive tests. However, before beginning the test and calibration procedures, analyze the problem and compare it to the symptoms discussed below. It may be possible to limit the repair to one or two PCBs or subassemblies.

Table 2: Troubleshooting Chart

Symptom	Solution
The liquid crystal display has no characters on it and the LEDs do not light.	Check all external power connections and sources. Check the fuses. Check all internal power supply voltages. Verify the 26-pin ribbon cable from the Front Panel I/O PCB is properly installed. Verify the 16-pin ribbon cable from the Front Panel I/O PCB to the liquid crystal display is properly installed. It is also possible there is a problem with the Data Processor PCB.
The LCD has characters on it and the LEDs are on, but the information is not meaningful.	There may be a problem with the LCD, the Front Panel PCB or the Data Processor PCB.

Table 2: Troubleshooting Chart

Symptom	Solution
When power is turned on, the LCD indicates that there is a problem with the RAM or EPROM on the Data Processor PCB.	The Data Processor may have a problem.
When power is turned on, the LCD indicates that there is a problem with the Signal Processor.	Test the Signal Processor and Signal Controller PCBs.
When power is turned on, the LCD shows the message, "Waiting For Signal Processor", longer than 10 seconds.	The Signal Controller PCB and/or the Signal Processor PCB may be malfunctioning. Run the tests on these boards.
The receiver will not track satellites.	Verify that the antenna is installed properly and the antenna cable is securely connected to the antenna and to the ANTENNA input on the Antenna Interface PCB. Verify that there are satellites visible (refer to Section 3). There could be a problem with the Antenna Interface PCB, the Signal Processor PCB or the Oscillator PLL. If it is possible that the antenna was not connected to the receiver when power was applied, make sure that it is connected, then cycle power to the receiver.
There is no output from the Output Buffer module.	The Output Buffer module is bad or there is a problem with the Oscillator Control Card. Verify that the 0.1 MHz, 1 MHz, 5 MHz, 10 MHz output has not been turned off (refer to Section 3).
The receiver does not indicate that the external 1 pps or the external reference is connected to the Input Buffer module.	External 1 pps and/or external reference is not connected, or the Input Buffer module is not working.

If spare PCBs and modules are available, the problem can be corrected quickly by replacing the bad component with the spare. The bad component can be repaired later when it is more convenient, or at the factory.

2.3. Cautions And General Procedures

The following paragraphs outline general procedures for testing and calibrating the Model 2201A GPS Satellite Receiver. A general discussion of the receiver hardware is also included. The following notes also apply.

☞ **NOTES:** 1. "Logic level", for use in this document, is defined as:
a. logic high, 2.4 V min for TTL and LSTTL,
b. logic high, 3.8 V min for HCMOS,
c. logic low, 0.5 V max for TTL and LSTTL,
d. logic low, 0.4 V max for HCMOS.

2. Unless otherwise specified, all data is taken at a nominal temperature of 21°C to 25°C and an input voltage of 117 Vac ±5% at 60 Hz.

2.3.1. Cautions

CAUTION: Line voltages are present in the left rear section of the chassis (transformer, ac fuse, and ac connector). While working in this area care should be taken to avoid electrical shock. Unless voltage measurements are being made, the power cord must be removed before repairing or replacing components in this area.

Disconnect all power to the receiver before removing or installing PCBs or cables. Failure to do so may result in damage to the components.

2.3.2. Brief Hardware Description

The Model 2201A consists of seven main areas, including eight plug-in boards, ac-to-dc power section, the front panel assembly and the option-module section. The front panel assembly consists of the panel and two PCBs. To remove the assembly from the chassis, first remove the two screws in the top corners of the panel, then tilt the panel outward. Disconnect the 26-pin ribbon cable from the Front Panel board and lift the panel out of the groove in the bottom crossbar. It is reinstalled by reversing this procedure. The bracket on the back of the panel pushes against the top edges of the three large PCBs (refer to next paragraph) to prevent them from being jarred loose in shipment.

The three large PCBs go in the center section behind the front panel. They can be installed in any order for testing. During testing, the board-under-test is installed in the top slot for convenience. The preferred order for normal operation is as follows:

1) Data Processor (10312798) in the top slot
2) Signal Controller (10310952) in the second slot
3) Signal Processor (10310873) in the third slot

The front left section of the chassis contains the DC-to-DC Converter assembly. This assembly plugs into the small connector on the Interconnect PCB, and is secured to the side panel by the thumbscrew on the heatsink. The assembly should be firmly attached to the side panel while power is on.

The Oscillator Control Card is plugged into the Interconnect PCB in the right front section of the chassis.

The left rear section of the chassis, as viewed from the front, contains the main power supply. This includes the ac-to-dc power supply, the external dc input, the ac fuse, and the dc circuit breakers.

The center section at the rear of the chassis has slots for the optional input/output modules (top two slots, any order) and the Antenna Input module (bottom slot). These modules are secured to the rear panel by two thumbscrews. A keying-hole in the bottom right corner keeps modules which do not belong there from being accidentally installed and possibly damaged when power is applied. Before shipping the receiver with these modules installed, the two thumbscrews should be tightened.

The main option slots are located in the right rear section of the chassis, as viewed from the front. These three slots will accept any combination, in any order, of several different option modules. These slots are also keyed. Modules that may be plugged into these four slots have a keying-hole in the bottom left corner. Before shipping the receiver with any of these modules installed, the two thumbscrews must be tightened.

The top and bottom covers slide in grooves in the side panels and are secured by two screws at the rear.

2.4. Recommended Test Equipment

The following equipment is recommended for testing and calibrating the Model 2201A. Where specific manufacturers model numbers are given, equivalent or better instruments may be substituted.

1) Multimeter
2) Multimeter, Systron/Donner Model 720
3) Oscilloscope, Tektronix Model 2445
4) Synthesizer, HP Model 3325A
5) DC power supply, 0-60 volts, 4 amperes, current limited

2.5. Receiver Tests

This section describes the tests and calibrations which must be performed on the Model 2201A GPS Receiver to ensure proper operation. Most tests and calibrations require some knowledge of the operation of the unit. It is recommended that you familiarize yourself with the manual before beginning these procedures.

2.5.1. Power Supply Tests

Verify the ac fuse is installed and the two dc circuit breakers have not tripped.

1) DC Circuit Breakers, 5 amps ("5" shown on button).
2) AC Fuse, 0.75 amp at 115 V.

Remove the top cover. Connect the multimeter LO input to test point TP4 on the DC-to-DC Converter Module, (P/N 23310989). Connect the receiver to a suitable power source. Measure the voltages at the following locations:

1) TP1 on DC-to-DC Converter, P/N 23310989. Adjust R1 for 5.0 Vdc, ±0.1 V.

2) TP3 on DC-to-DC Converter, P/N 23310989. Adjust R4 for –15.0 Vdc, ±0.2 V.

3) TP2 on DC-to-DC Converter, P/N 23310989. Adjust R2 for 15.0 Vdc, ±0.2 V.

4) TP5 on DC-to-DC Converter, P/N 23310989. Adjust R6 for 24.0 Vdc, ±0.2 V.

5) Pin 26 of XA5. Adjust R1 on the Main Interconnect PCB (P/N 10310751) for 5.0 Vdc, ±0.1 V.

2.5.2. Front Panel I/O Tests, P/N 10911118

Connect the receiver to a suitable power source and verify that the display performs as described in the manual for start-up. If all dots are off or all dots are on, do the following before trouble shooting the circuits. Make the following adjustment while looking at the display straight on:

1) Adjust potentiometer, R2, until all dots appear to be on. Gradually reverse the adjustment until the STARTUP display is visible.

2) Continue the adjustment until the OFF DOTS are just barely visible.

The purpose of this adjustment is to obtain the best contrast possible. When the adjustment is done, continue with the Front Panel tests. If the start-up display is not visible, no matter what setting of R2, the cable to the Front Panel may not be connected or there is a problem with the circuits on the Front Panel PCB. Do not continue with the Front Panel tests until the start-up display is visible.

To enable the receiver tests, press [MENU], then [ESC] to return to the main screen. Press the following sequence of keys: [ALT], [9], [EE], [CE], [ESC]. Press [MENU], then select Initialization, Receiver Setup, Receiver Tests, and Front Panel. The following screen is displayed.

```
FRONT PANEL

1)Keypad/LCD
2)LEDs
```

Next, select Keypad/LCD. This selection causes the display to go completely blank. Beginning with the [MENU] button, push each button in order, (except for [ESC]) moving left-to-right and top-to-bottom. When a button is pushed, verify that all character positions of the LCD show the character associated with that button. The following table shows the character which must be displayed when a key is pushed. It also shows the hex value associated with each key.

Table 3: Keypad/LCD Test		
KEY NAME	DISPLAYED CHARACTER	HEX VALUE
Menu	(all dots on)	0F
±	+	0B
7	7	07
8	8	08
9	9	09
ENT	E	0E
ESC	(return to Menu)	10
.	.	0A
4	4	04
5	5	05
6	6	06
CE	C	0D
ALT	A	11
0	0	00
1	1	01
2	2	02
3	3	03
EE	(all dots off)	0C

If a key causes no response, or if the wrong character is displayed, fix the problem before continuing. When all keys and the LCD have been checked, press [ESC] to return to the FRONT PANEL submenu.

From the FRONT PANEL submenu, select the LED test. The POWER LED should always be green, and the ALARM and 1 pps LEDs should be off. Use the keys, as shown in the table below, to turn on a particular LED (the 1 pps LED flashes at a 1 pps rate in the color selected).

LED	KEY
ALARM-RED	1
ALARM-GREEN	2
1 PPS-RED	3
1 PPS-GREEN	4

Only one LED at a time should be on. When the LEDs work properly, return to the main menu by pressing [MENU], then [ESC]. This completes the Front Panel Assembly tests.

2.5.3. Data Processor Calibration, P/N 10312798

Check the EPROMs and all other ICs that are in sockets for bent pins. If it is not already there, install the Data Processor in the top slot of the receiver. Move all other boards down to slots 2 and 3.

When the main screen is displayed, press the following sequence of keys to enable the receiver tests: [ALT], [9], [EE], [CE], [ESC]. Press [MENU], then select Initialization, Receiver Setup, and Receiver Tests. Select Signal Ctrl/Proc, then enable these tests by pressing [1] (Enable Tests). The following screen appears for approximately five seconds.

```
SIGNAL CTRL/PROC

     Please wait, enabling Test Setup
```

After the delay, the following screen is displayed.

```
SIGNAL CTRL/PROC
1)Disable Tests      4)1PPS Cal
2)IRQ Latch          5)A/D CHECK
3)C/A CLOCK          6)AGC
```

Select IRQ Latch, to test (U10). The following screen is displayed.

```
LATCH

Trigger scope on U10-11
Verify pulses at U10-12,13,14,15,16,17
```

Trigger oscilloscope channel A with the falling edge of the pulse at (U10,11). On channel B, check the following pins in the order shown for a positive-going pulse:

U10 pin 12
pin 13
pin 14
pin 15
pin 16
pin 17

Terminate the test by pressing [ESC]. This completes the Signal Controller test.

Turn power on and verify that the LCD performs as described in the manual for start-up. If it does not, check the following pins of the MPU (U18) on the Data Processor:

1) Pin 14: 5 Vdc (Vcc)
2) Pin 15: 10 MHz clock (TTL, MPU clock)
3) Pin 16: ground (Vss)
4) Pin 17: 5 Vdc ($\overline{\text{HALT}}$)
5) Pin 18: 5 Vdc ($\overline{\text{RESET}}$)
6) Pin 49: 5 Vdc (Vcc)
7) Pin 53: ground (Vss)

When the start-up display is correct, continue with the Data Processor calibration.

To enable the receiver tests, press the following sequence of keys while the main screen is displayed: [ALT], [9], [EE], [CE], [ESC]. Press [MENU], then select Initialization, Receiver Setup, Receiver Tests, and Data Processor. This begins the calibration of the time interval counter on this board. The following screen appears.

```
TIC CALIBRATION
Start High = 239      Stop High = 241
Start Low  = 175      Stop Low  = 175
Slope      = 650      Slope     = 660
```

Connect an oscilloscope to (U25,16) and adjust potentiometer R9 for 0.0 V ±0.050 V. Connect the oscilloscope to (U20,16) and adjust R20 for 0.0 V ±0.05 V.

While looking at the TIC CALIBRATION screen, adjust R6 to give a START HIGH of 240 ±5. Adjust R16 to give a STOP HIGH of 240 ±5. The Start Slope and the Stop Slope should be at least 550.

This completes the calibration of the Data Processor PCB. Turn the receiver OFF before continuing with the next test.

2.5.4. Signal Controller Tests, P/N 10310952

With power off, install the Signal Controller in the top slot of the receiver with the Signal Processor PCB (P/N 10310873) in the next slot. Use the following procedure to do this. First, remove the Front Panel assembly. Then, remove the 40-pin ribbon cable from the Signal Controller and Signal Processor PCBs. Place the Signal Controller in the top slot and the Signal Processor in the second slot. Reconnect the 40-pin ribbon cable to both PCBs. The Data Processor board should be installed in the third slot from the top. Reinstall the Front Panel assembly.

Connect ac power. The main screen should come up within 15 seconds. If this does not happen, check all connections (ICs in sockets, cables, etc.) and if they look okay, pull the board and give it a good visual inspection.

2.5.5. Signal Processor Tests, P/N 10310873

Before testing this PCB, make sure that all socketed ICs are installed properly, especially (U18). IC (U18), ST1172, is a very expensive CMOS IC and it must be handled carefully. If it is thought to be bad, remove it carefully from it's socket and press it into a piece of conductive foam. Try a replacement IC. If the new IC works, the old one may be bad. If the new IC does not work, the problem is probably elsewhere.

Install the Signal Processor PCB in the top slot of the receiver. Install the Signal Controller PCB (P/N 10310952) in the second slot and connect the ribbon cable from the Signal Processor to the Signal Controller. Connect ac power to the receiver.

Initialize the Signal Processor as follows: place jumpers on W1-B and W2-B. Adjust R1, R16, R17, and R46 fully COUNTERCLOCKWISE, and adjust C38 fully CLOCKWISE. With the receiver displaying the main screen, press the following sequence of keys to enable the Receiver Tests: ALT-9-EE-CE-ESC. Press MENU, then select Initialization, Receiver Setup, Receiver Tests, and Signal Ctrl/Proc. Select Enable Tests to enable the Signal Processor tests.

Use a frequency counter or oscilloscope to verify the presence of the following signals. Connect the counter ground to the grounded side of C82.

1) (U19,9) 1 kHz square wave, ±10 Hz
2) (U4,38) 62.5 kHz square wave, ±100 Hz
3) (U4,37) 5.00 kHz square wave, ±25 Hz
4) (U4,7) 2.5 MHz square wave, ±1 kHz
5) (U18,14) 80.0 kHz signal, ±200 Hz
6) (U18,15) 80.0 kHz signal, ±200 Hz

Verify that C38 has been adjusted fully CLOCKWISE, then back it out 3.5 turns. W2-B must be closed. Connect a frequency counter to (U12,4) and measure the frequency. It should be 10.23 MHz, ±100 Hz. If it is more than 100 Hz high, change C34 to 82pF (605110-0820). If it is more than 100 Hz low, change C34 to 56pF (605110-0560).

Change jumper W2 from B to A. Connect the frequency counter to (U12,4). For best results with this measurement, connect the external reference input of the counter to the "0.1, 1, 5, 10 MHz" output on the Output Buffer module (or any output module installed). If necessary, follow the instructions in the manual supplement (P/N 12712120) to change the frequency of this module output to the frequency required by the counter (terminate the output of the receiver with 50 Ω at the input of the counter). The frequency of the signal at (U12,4) should be 10.23 MHz ±2 Hz.

Connect a voltmeter to the intersection of R25 and L1 and adjust C38 to give a voltage of 4.5 Vdc ±0.2 volt. If it is necessary to turn C38 more than one turn in either direction, repeat the calibration of C38 and C34, described above.

Return to the SIGNAL CTRL/PROC submenu and select C/A CLOCK. Make sure that R46 is fully COUNTERCLOCKWISE. Trigger the oscilloscope on the rising edge of the signal at (U13-10). Set the oscilloscope timebase to 0.2 µsec/division and select X10. Also, set the channel 2 vertical to 1 volt/division.

While still triggering the oscilloscope as described above, look at the signal at (U24-10) on channel 2. Center on the graticule, the first pair of falling edges on channel 2. As R46 is adjusted

CLOCKWISE, the left falling edge (the moving edge) moves to the right on the graticule. When the two falling edges are approximately 1 cm apart, set the timebase to 0.1 µsec/division (X10 still selected). Recenter the first pair of falling edges on the graticule. Continue to adjust R46 CLOCKWISE until the moving edge is 4 nanoseconds to the left of the stationary edge. Measure the separation at the middle (vertically) of the signal. **Do not allow the moving edge to go to the right of the stationary edge.**

Return to the SIGNAL CTRL/PROC submenu and select 1PPS CAL. Make sure that R1 is fully COUNTERCLOCKWISE. Trigger the oscilloscope on the rising edge of the signal at (U13-12). Set the oscilloscope timebase to 0.2 µsec/division and select X10. Also, set the channel 2 vertical to 1 volt/division.

While still triggering the oscilloscope as described above, look at the signal at (U22-6) on channel 2. Center on the graticule, the first pair of falling edges on channel 2. As R1 is adjusted CLOCKWISE, the left falling edge (the moving edge) moves to the right on the graticule.

When the two falling edges are approximately 1 cm apart, set the timebase to 0.1 µsec/division (X10 still selected). Recenter the first pair of falling edges on the graticule. Continue to adjust R1 CLOCKWISE until the moving edge is 2 nanoseconds to the left of the stationary edge. Measure the separation at the middle (vertically) of the signal. **Do not allow the moving edge to go to the right of the stationary edge.**

Return to the SIGNAL CTRL/PROC submenu and select A/D CHECK. Make sure that W1-B is closed, and that R16 and R17 are fully COUNTERCLOCKWISE. The following screen appears.

```
A/D CHECK
                IVAL = xxxx
                QVAL = yyyy
                DIFF = zzzz
```

This screen shows the current value of A/D converter (U26) as IVAL = xxxx, the current value of A/D converter (U27) as QVAL = yyyy, and the difference between these two values as DIFF = zzzz. IVAL and QVAL can have maximum values of –2047. The minimum value will typically be in the range of –5 to +5.

Adjust R16 CLOCKWISE, slowly. Verify that xxxx and yyyy decrease, and that zzzz stays equal to or less than 9. Observe the display while R16 is adjusted through its entire range. When this test is completed, leave R16 fully CLOCKWISE, and adjust R17 fully CLOCKWISE. Close W1-A.

Return to the SIGNAL CTRL/PROC submenu. Verify that W1-A is closed and that R17 is fully CLOCKWISE. Remove power from the receiver and unplug the Antenna Interface module (P/N 23411147). Connect AC power to the receiver. Connect the synthesizer to the end of R2 that is connected to P1-85,86. Set the synthesizer for 80 kHz, 0.0 Vdc offset and 0.5 Vp-p (terminate the output of the synthesizer so that its output is calibrated, or look at the output on an oscilloscope and adjust the synthesizer output level to give 0.5 Vp-p).

Select AGC from the SIGNAL CTRL/PROC screen. While looking at (U9,2) with an oscilloscope, enter an AGC value of 255 and adjust R17 to give an output of 10.0 Vp-p. Set the AGC to the following values and verify that the output is approximately half the previous value.

AGC VALUE	Vp-p
128	5.0, ±0.5
64	2.5, ±0.5
32	1.25, ±0.25
16	0.625, ±0.125
8	0.31, ±0.0625
4	0.16, ±0.03
2	0.08, ±0.015

When this test is completed, turn R17 fully CLOCKWISE, disconnect the synthesizer, and plug the Antenna Interface module in (remove power before plugging the module in).

This completes the test and calibration of the Signal Processor PCB.

2.5.6. Antenna Interface Module Tests, P/N 23411147

Remove all jumpers from the headers on the board.

☞ **NOTE**: The following labels will be used to denote the jumpers to be used in this test:

LABEL	LOCATION
W1-1	Connects to (U12-3,4)
W1-2	Connects to C17
W2-1	Connects to C20
W3-1	Connects to (U1,6)
W4-1	Connects to C24
W5-1	Connects to L15

Place jumpers on W6-B and W7. Install the module in the top slot of the middle section of the rear panel. Turn power ON.

Set the synthesizer to output an 80 kHz sine wave at 32 mVp-p; do not terminate the synthesizer for this test. Connect the synthesizer to W3-1 (the pin closest to the card edge-connector). At (U1,12) there should be an 80 kHz sine wave, with an amplitude of 10 Vp-p ±1.0 V (use the oscilloscope).

Verify that the 3 dB bandwidth of the signal at (U1,12) is greater-than-or-equal-to ±10 kHz. Use the following procedure to do this:

1) Using the oscilloscope Vertical Adjust (uncalibrated, if necessary), set the 80 kHz signal so that it swings full-scale on the graticule (8 divisions, peak-to-peak). Set the time base to 1 millisecond/cm.

2) Slowly lower the frequency output of the synthesizer from 80 kHz until the signal level is approximately 5.6 divisions peak-to-peak. This is the lower 3 dB frequency. Record it.

3) Return the synthesizer to 80 kHz.

4) Slowly raise the frequency output of the synthesizer from 80 kHz until the signal level is approximately 5.6 divisions peak-to-peak. This is the upper 3 dB frequency. Record it.

5) Subtract the lower frequency from the upper frequency to get the 3 dB bandwidth of the filter. It should be greater- than-or-equal-to 10 kHz.

When the calibration is complete, disconnect the synthesizer from W3-1. Set the synthesizer to generate a 14.58 MHz sine wave at a level of –32 dBm. Connect the synthesizer to W1-2 (pin connected to C17). Connect an oscilloscope to W2-1 (pin connected to C20) and adjust C22, C23, C11 and C12 (in that order) for maximum level of the 14.58 MHz signal. Repeat these adjustments three times to make sure that maximum signal is obtained. The output should be at least 0.20 Vp-p when the adjustments are complete.

Set the synthesizer to scan from 14.57 MHz to 4.59 MHz with a time of .01 second, then start the scan. Trigger the oscilloscope on the negative-going edge of the synthesizer's Z BLANK output. Adjust the oscilloscope timebase to 1 ms/cm (2 kHz/cm). Observe the signal envelope at W2-1 on the oscilloscope and expand the amplitude of the display (10 mV range). Using the Uncal, adjust the signal envelope for full scale. Detune C12 to give a 3 dB bandwidth of at least ±6.0 kHz, but no greater than ±8 kHz. Adjust the signal envelope to be as symmetrical as possible. When adjustment is complete, remove the synthesizer.

Connect a spectrum analyzer to W4-1 (center pin), using the special shielded coax cable. Set the analyzer for a frequency of 90 MHz, a scan width of 2 MHz/cm, and a bandwidth of 100 kHz. Adjust R14 for the best null of the carrier at 90 MHz. it should be at least 20 dB below the first 500 kHz sidebands. Reinstall W4-B.

Remove W8 and connect a frequency generator to Antenna Input, J1. Set the frequency of the generator to 75.42 MHz ±2 kHz; set its output level to –30 dBm using a spectrum analyzer. Connect an oscilloscope to W1-1, pin connected to (U12,3), and verify that the 75.42 MHz is at least 0.3 Vp-p.

Using an oscilloscope, check for the presence of the following signals:

1) 10 MHz sine wave at W5-1, at least 0.2 Vp-p

2) 15 MHz TTL level square wave at (U6,8)

3) 500 kHz, distorted signal at (U5,13)

Turn the receiver power OFF. Place jumpers on W1-W3 and W4-B. Remove jumpers W6-A, W6-B, and W7.

Turn power on. Connect a frequency generator to J1. Set the level to –65 dBm and the frequency to 75.42 MHz ±2 kHz. Using an oscilloscope, verify the presence of an 80 kHz output at (U1,12) at a level of at least 0.5 Vp-p. Verify that the 3 dB passband is at least ±4.5 kHz (centered around 80 kHz) by varying the frequency of the generator (use a procedure similar to the procedure described above). The frequency change at (U1,12) is equal to the frequency change at J1.